18.4.6.11 Slot time

The slot time for the High Rate PHY shall be the sum of the RX-to-TX turnaround time (5 μs) and the energy detect time (15 μs specified in 18.4.8.4). The propagation delay shall be regarded as being included in the energy detect time.

18.4.6.12 Channel switching/settling time

When the Channel Agility option is enabled, the time to change from one operating channel frequency to another, as specified in 18.4.6.2, is 224 μs. A conformant PMD meets this switching time specification when the operating channel center frequency has settled to within ±60 kHz of the nominal channel center. Stations shall not transmit until after the channel change settling time.

18.4.6.13 Transmit and receive antenna port impedance

The impedance of the transmit and receive antenna port(s) shall be 50 Ω if the port is exposed.

18.4.6.14 Transmit and receive operating temperature range

Two temperature ranges are specified for full operation compliance to the High Rate PHY. Type 1 shall be defined as 0 °C to 40 °C, and is designated for office environments. Type 2 shall be defined as –30 °C to +70 °C, and is designated for industrial environments.

18.4.7 PMD transmit specifications

Subclauses 18.4.7.1 through 18.4.7.8 describe the transmit functions and parameters associated with the PMD sublayer.

18.4.7.1 Transmit power levels

The maximum allowable output power, as measured in accordance with practices specified by the appropriate regulatory bodies, is shown in Table 115. In the USA, the radiated emissions should also conform with the ANSI uncontrolled radiation emission standards (IEEE Std C95.1-1999).

Table 115—Transmit power levels

Maximum output power	Geographic location	Compliance document
1000 mW	USA	FCC 15.247
100 mW (EIRP)	Europe	ETS 300–328
10 mW/MHz	Japan	MPT ordinance for Regulating Radio Equipment, Article 49-20

18.4.7.2 Transmit power level control

Power control shall be provided for transmitted power greater than 100 mW. A maximum of four power levels may be provided. As a minimum, a radio capable of transmission greater than 100 mW shall be capable of switching power back to 100 mW or less.

18.4.7.3 Transmit spectrum mask

The transmitted spectral products shall be less than –30 dBr (dB relative to the SINx/x peak) for

f_c – 22 MHz < f < f_c –11 MHz; and
f_c + 11 MHz < f < f_c + 22 MHz;

and shall be less than –50 dBr for

f < f_c – 22 MHz; and
f > f_c + 22 MHz.

where

f_c is the channel center frequency.

The transmit spectral mask is shown in Figure 145. The measurements shall be made using a 100 kHz resolution bandwidth and a 100 kHz video bandwidth.

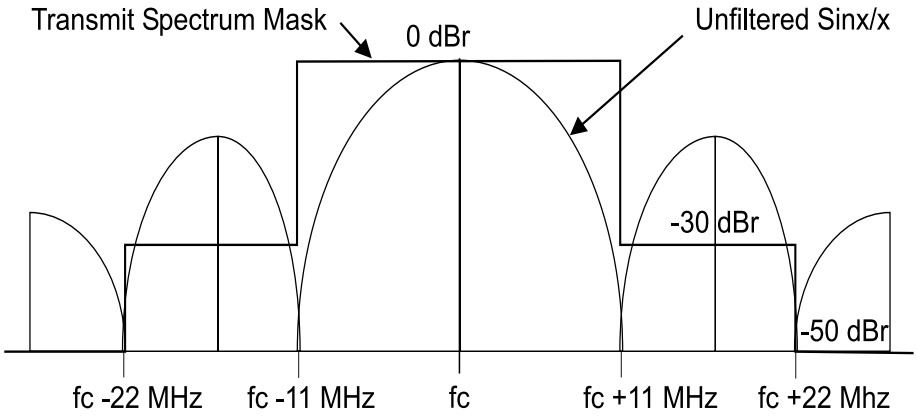

Figure 145—Transmit spectrum mask

18.4.7.4 Transmit center frequency tolerance

The transmitted center frequency tolerance shall be ±25 ppm maximum.

18.4.7.5 Chip clock frequency tolerance

The PN code chip clock frequency tolerance shall be better than ±25 ppm maximum. It is highly recommended that the chip clock and the transmit frequency be locked (coupled) for optimum demodulation performance. If these clocks are locked, it is recommended that bit 2 of the SERVICE field be set to a 1, as indicated in 18.2.3.4.

18.4.7.6 Transmit power-on and power-down ramp

The transmit power-on ramp for 10% to 90% of maximum power shall be no greater than 2 μs. The transmit power-on ramp is shown in Figure 146.

The transmit power-down ramp for 90% to 10% maximum power shall be no greater than 2 μs. The transmit power-down ramp is shown in Figure 147.

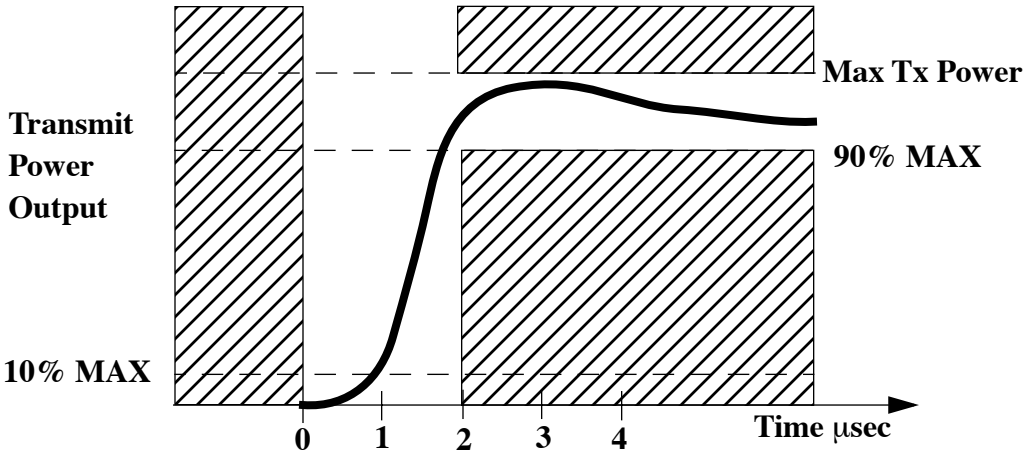

Figure 146—Transmit power-on ramp

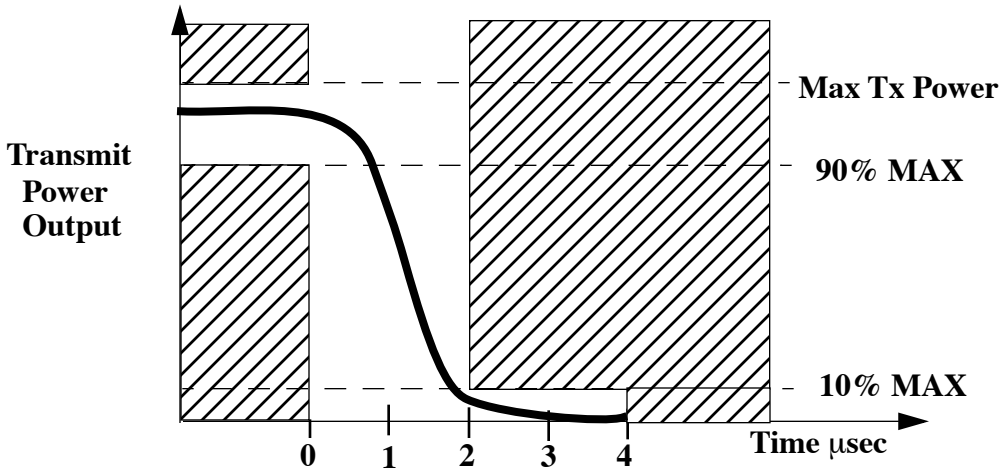

Figure 147—Transmit power-down ramp

The transmit power ramps shall be constructed such that the High Rate PHY emissions conform with spurious frequency product specification defined in 18.4.6.8.

18.4.7.7 RF carrier suppression

The RF carrier suppression, measured at the channel center frequency, shall be at least 15 dB below the peak SIN(x)/x power spectrum. The RF carrier suppression shall be measured while transmitting a repetitive 01 data sequence with the scrambler disabled using DQPSK modulation. A 100 kHz resolution bandwidth shall be used to perform this measurement.

18.4.7.8 Transmit modulation accuracy

The transmit modulation accuracy requirement for the High Rate PHY shall be based on the difference between the actual transmitted waveform and the ideal signal waveform. Modulation accuracy shall be determined by measuring the peak vector error magnitude during each chip period. Worst-case vector error magnitude shall not exceeded 0.35 for the normalized sampled chip data. The ideal complex I and Q constellation points associated with DQPSK modulation, (0.707,0.707), (0.707, –0.707), (–0.707, 0.707), (–0.707, –0.707), shall be used as the reference. These measurements shall be from baseband I and Q sampled data after recovery through a reference receiver system.

Figure148 illustrates the ideal DQPSK constellation points and range of worst-case error specified for modulation accuracy.

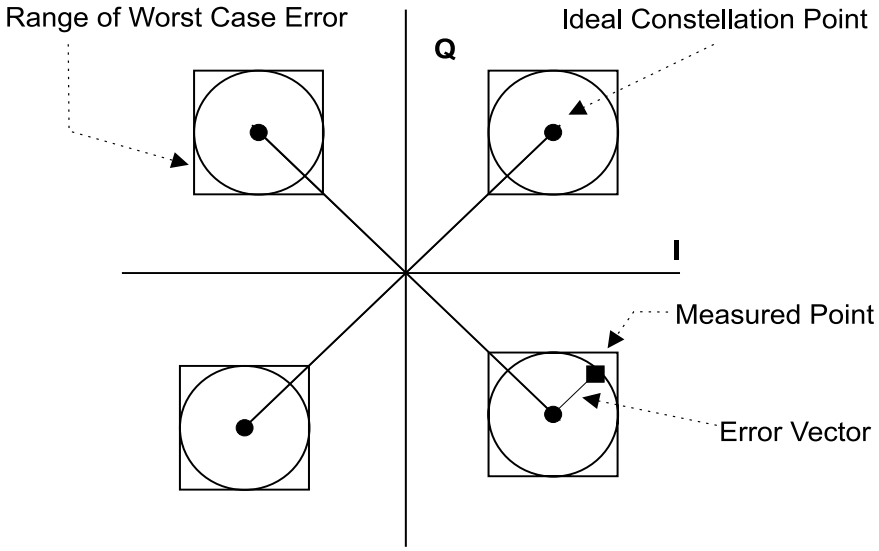

Figure 148—Modulation accuracy measurement example

Error vector measurement requires a reference receiver capable of carrier lock. All measurements shall be made under carrier lock conditions. The distortion induced in the constellation by the reference receiver shall be calibrated and measured. The test data error vectors described below shall be corrected to compensate for the reference receiver distortion.

The IEEE 802.11-compatible radio shall provide an exposed TX chip clock, which shall be used to sample the I and Q outputs of the reference receiver.

The measurement shall be made under the conditions of continuous DQPSK transmission using scrambled all one's.

The eye pattern of the I channel shall be used to determine the I and Q sampling point. The chip clock provided by the vendor radio shall be time delayed, such that the samples fall at a 1/2 chip period offset from the mean of the zero crossing positions of the eye (see Figure 149). This is the ideal center of the eye and may not be the point of maximum eye opening.

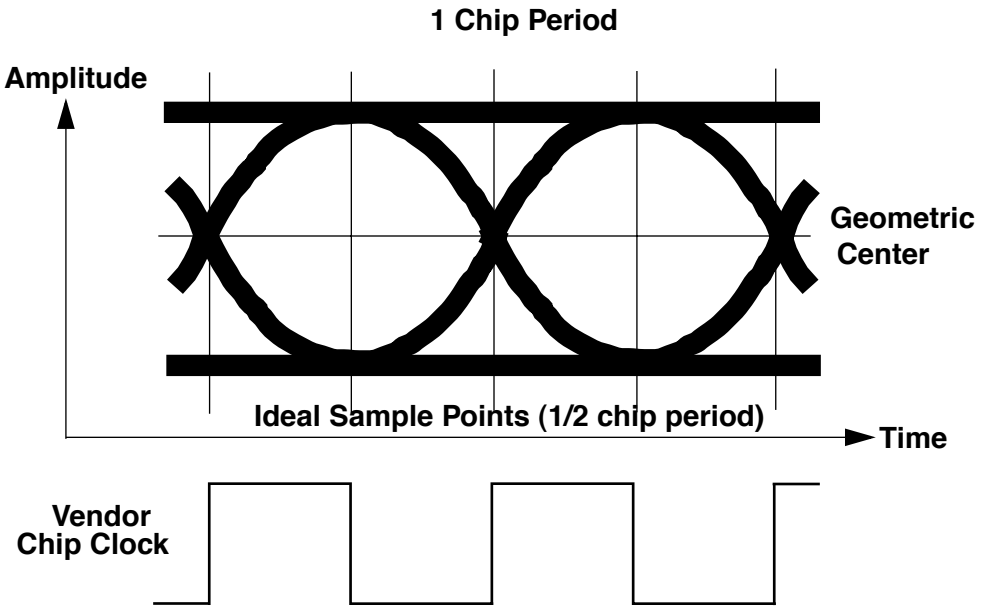

Figure 149—Chip clock alignment with baseband eye pattern

Using the aligned chip clock, 1000 samples of the I and Q baseband outputs from the reference receiver are captured. The vector error magnitudes shall be calculated as follows:

Calculate the dc offsets for I and Q samples

$$I_{\text{mean}} = \sum_{n=0}^{999} I(n) / 1000$$

$$Q_{\text{mean}} = \sum_{n=0}^{999} Q(n) / 1000$$

Calculate the dc corrected I and Q samples for all n = 1000 sample pairs

$I_{dc}(n) = I(n) - I_{mean}$

$Q_{dc}(n) = Q(n) - Q_{mean}$

Calculate the average magnitude of I and Q samples

$$I_{\text{mag}} = \sum_{n=0}^{999} |I_{\text{dc}}(n)| / 1000$$

$$Q_{\text{mag}} = \sum_{n=0}^{999} |Q_{\text{dc}}(n)| / 1000$$

Calculate the normalized error vector magnitude for the $I_{dc}(n)/Q_{dc}(n)$ pairs

$$V_{\text{err}}(n) = \left[\frac{1}{2} \times (\{|I_{\text{dc}}(n)| - I_{\text{mag}}\}^2 + \{|Q_{\text{dc}}(n)| - Q_{\text{mag}}\}^2)\right]^{\frac{1}{2}} - V_{\text{correction}}$$

where

$V_{correction}$ is the error induced by the reference receiver system.

A vendor High Rate PHY implementation shall be compliant if for all n = 1000 samples, the following condition is met:

$V_{err}(n) < 0.35$

18.4.8 PMD receiver specifications

Subclauses 18.4.8.1 through 18.4.8.4 describe the receive functions and parameters associated with the PMD sublayer.

18.4.8.1 Receiver minimum input level sensitivity

The frame error ratio (FER) shall be less than 8×10^{-2} at a PSDU length of 1024 octets for an input level of –76 dBm measured at the antenna connector. This FER shall be specified for 11 Mbit/s CCK modulation. The test for the minimum input level sensitivity shall be conducted with the energy detection threshold set less than or equal to –76 dBm.

18.4.8.2 Receiver maximum input level

The receiver shall provide a maximum FER of 8×10^{-2} at a PSDU length of 1024 octets for a maximum input level of –10 dBm measured at the antenna. This FER shall be specified for 11 Mbit/s CCK modulation.

18.4.8.3 Receiver adjacent channel rejection

Adjacent channel rejection is defined between any two channels with ≥25 MHz separation in each channel group, as defined in 18.4.6.2.

The adjacent channel rejection shall be equal to or better than 35 dB, with an FER of 8×10^{-2} using 11 Mbit/s CCK modulation described in 18.4.6.3 and a PSDU length of 1024 octets.

The adjacent channel rejection shall be measured using the following method.

Input an 11 Mbit/s CCK modulated signal at a level 6 dB greater than specified in 18.4.8.1. In an adjacent channel (≥ 25 MHz separation as defined by the channel numbering), input a signal modulated in a similar fashion, which adheres to the transmit mask specified in 18.4.7.3, to a level 41 dB above the level specified in 18.4.8.1. The adjacent channel signal shall be derived from a separate signal source. It cannot be a frequency shifted version of the reference channel. Under these conditions, the FER shall be no worse than 8×10^{-2}.

18.4.8.4 CCA

The High Rate PHY shall provide the capability to perform CCA according to at least one of the following three methods:

— CCA Mode 1: Energy above threshold. CCA shall report a busy medium upon detecting any energy above the ED threshold.

— CCA Mode 4: Carrier sense with timer. CCA shall start a timer whose duration is 3.65 ms and report a busy medium only upon the detection of a High Rate PHY signal. CCA shall report an IDLE medium after the timer expires and no High Rate PHY signal is detected. The 3.65 ms timeout is the duration of the longest possible 5.5 Mbit/s PSDU.

— CCA Mode 5: A combination of carrier sense and energy above threshold. CCA shall report busy at least while a High Rate PPDU with energy above the ED threshold is being received at the antenna.

The energy detection status shall be given by the PMD primitive, PMD_ED. The carrier sense status shall be given by PMD_CS. The status of PMD_ED and PMD_CS is used in the PLCP convergence procedure to indicate activity to the MAC through the PHY interface primitive, PHY-CCA.indicate.

A busy channel shall be indicated by PHY-CCA.indicate of class BUSY. A clear channel shall be indicated by PHY-CCA.indicate of class IDLE.

The PHY MIB attribute, dot11CCAModeSupported, shall indicate the appropriate operation modes. The PHY shall be configured through the PHY MIB attribute, dot11CurrentCCAMode.

The CCA shall indicate TRUE if there is no energy detect or carrier sense. The CCA parameters are subject to the following criteria:

a) If a valid High Rate signal is detected during its preamble within the CCA assessment window, the energy detection threshold shall be less than or equal to –76 dBm for TX power > 100 mW; –73 dBm for 50 mW < TX power ≤ 100 mW; and –70 dBm for TX power ≤ 50 mW.

b) With a valid signal (according to the CCA mode of operation) present at the receiver antenna within 5 μs of the start of a MAC slot boundary, the CCA indicator shall report channel busy before the end of the slot time. This implies that the CCA signal is available as an exposed test point. Refer to Figure 47 of IEEE Std 802.11, 1999 Edition for a slot time boundary definition.

c) In the event that a correct PLCP header is received, the High Rate PHY shall hold the CCA signal inactive (channel busy) for the full duration, as indicated by the PLCP LENGTH field. Should a loss of carrier sense occur in the middle of reception, the CCA shall indicate a busy medium for the intended duration of the transmitted PPDU. Upon reception of a correct PLCP header, the timer of CCA Mode 2 shall be overridden by this requirement.

Conformance to the High Rate PHY CCA shall be demonstrated by applying an equivalent High Rate compliant signal above the appropriate ED threshold (item a), such that all conditions described in items (b) and (c) above are demonstrated.

